Amendments to the Specification

Please substitute the following paragraphs/sections for the pending paragraphs/sections.

Please substitute paragraph 9 with the following paragraph:

B1

The gate capacitance is inversely proportional to the thickness of the gate oxide. As the technology advances, the thickness of the gate oxide of the transistor decreases, thus increasing the capacitance. However, a decrease of the gate oxide thickness causes the leakage current through the ~~agate~~ gate to increase. In the LPF 112 of the PLL circuit in FIG. 1, the gate voltage across the capacitor is used to control the VCO 114, which outputs the desired frequency SVCO. If there is gate leakage in the PMOS FET capacitor, the control voltage will not be held constant and will cause drift in the output frequency of VCO 114.

Please substitute paragraph 10 with the following paragraph:

B2

What is needed is a technique to obtain a stable ~~a~~ PLL control voltage, without drastically increasing the complexity and cost of the circuit.

Please substitute paragraph 12 with the following paragraph:

B3

In another embodiment of the present invention, a low-pass filter for a phase locked loop (PLL) circuit includes a capacitor, comprising: an N-type substrate, a P-type region formed on the N-type substrate, a thick oxide formed over the P-type region, a P^+ gate electrode formed over the thick oxide and coupled to a first voltage supply line, and P^+ pick-up terminals formed in the P-type region adjacent the gate electrode and coupled to a second voltage supply line. A gate-to-substrate voltage is maintained at less than zero volts to maintain a stable control voltage for the PLL.

Please substitute paragraph 20 with the following paragraph:

B4

FIG. 6 is a plot of capacitance ~~verses~~ versus voltage (C-V) for a P-gate NMOS capacitor, according to an embodiment of the present invention.